



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,020	03/30/2004	Kang-seok Cho	1572.1312	2784

21171 7590 12/11/2006

STAAS & HALSEY LLP  
SUITE 700  
1201 NEW YORK AVENUE, N.W.  
WASHINGTON, DC 20005

EXAMINER
----------

BAE, JI H

ART UNIT	PAPER NUMBER
----------	--------------

2115

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/812,020	CHO, KANG-SEOK	
	<b>Examiner</b>	<b>Art Unit</b>	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 14 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,2,4 and 6-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4 and 6-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |                                                                                        |                                                                   |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11-3-2006</u> .                                               | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments, see page 1 of applicant's remarks, filed on 14 September 2006, with respect to rejection of claims 3, 5, and 9 have been fully considered and are persuasive. The rejection of claims 3, 5, and 9 has been withdrawn.

Applicant's arguments with respect to prior art based rejections have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 6-8, 11, 12, 14, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki, U.S. Patent No. 6,446,213 B1, in view of Watts, U.S. Patent No. 6,336,161 B1.

Claims 1, 2, 6, 9, 10, 13, 14, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki in view of Park, U.S. Patent Application Publication No. 2003/0145191 A1.

Regarding claim 1<sup>1</sup>, Yamaki teaches:

a system memory [Fig. 2, system memory 13];

Art Unit: 2115

a power management controller to control a supply power to the system [power supply controller 16];

and a controller to enable a power saving standby mode [EC 18], to control the power management controller to store an operating state stored in the system memory when the power saving standby mode is selected [col. 10, lines 37-47].

Yamaki does not teach storing the operating state to a flash memory and cutting off the power.

Watts and Park both teach storing the operating state of a computer to a flash memory and cutting off the power [Watts Fig. 3a, Park Fig. 3].

It would have been obvious to one ordinary skill in the art to combine the teachings of Yamaki and Watts by modifying Yamaki to store the operating state to a flash memory and to cut off the power. Both Watts and Yamaki are directed towards systems and methods of power management for computers. Watts teaches that power is completely removed from the system [col. 4, lines 66-67] instead of being maintained in a sleep mode. Since power is completely removed from the system, a greater power saving is achieved over a sleep mode. Additionally, Watts teaches that storing the operating state to a flash memory allows for quick return to the previous operating state [col. 2, lines 38-49]. The teaching of Watts would improve the system of Yamaki by providing these features.

Additionally, it would have been obvious to one of ordinary skill in the art to combine the teachings of Yamaki with Park. Both Yamaki and Park provide methods for saving the operating state of the computer prior to switching to a lower power mode. Yamaki teaches saving the operating state to a main memory and placing the computer in a sleep mode [col. 10, lines 37-47], while Park teaches saving to a flash memory and removing power from the system.

---

<sup>1</sup> Watts and Park cited in prior office action.

Art Unit: 2115

The flash memory of Park provides a number of advantages, including portability, and facilitating increased power saving by completely removing power from the system [paragraph 9]. The teachings of Park would improve the system of Yamaki by providing these features.

Regarding claim 2, Park teaches that the flash memory is connected to a USB port [paragraph 39].

Regarding claim 4, Watts teaches that the controller stores the operating state stored in the flash memory to the system memory when the power saving standby mode is changed to a normal mode in which normal operations are conducted [Fig. 3b, steps 64, 66].

Regarding claim 6, Yamaki/Park teaches a method comprising [Park Fig. 3]:

selecting a power saving standby mode [32];

storing an operating state stored in the system memory to a flash memory when the power saving standby mode is selected [36]; and

cutting power supply to the system after the operating state has been stored [paragraph 30].

Additionally, Yamaki teaches a power management controller to control a power supply [power supply controller 16].

Regarding claim 6, Yamaki/Watts teaches a method with steps comprising:

selecting a power saving standby mode [Fig. 3a, step 56];

storing an operating state stored in the system memory to a flash memory when the power saving standby mode is selected [steps 58, 60];

and cutting power supply to the system after the operating state has been stored [step 62].

Additionally, Yamaki teaches a power management controller to control a power supply [power supply controller 16].

Regarding claim 7, Watts teaches re-supplying power to the system when the power saving standby mode is changed to a normal mode in which normal operations are conducted and storing the operating state stored in the flash memory to the system memory [Fig. 3b].

Regarding claim 8, Watts teaches that the power saving standby mode is selected via a user interface [col. 4, lines 10-12].

Regarding claim 9, Park teaches selecting a standby mode or maximum power saving mode, checking whether the flash memory is connected to the system, and determining the selection when the flash memory is connected [Fig. 3, steps 34, 36, 38, paragraph 28 and 29].

Regarding claims 10 and 13, Park teaches a USB flash device [paragraph 39]; therefore the device is detachably provided to the computer system, and the USB port is used to restore/save from/to the flash memory device.

Regarding claims 11 and 15, it would have been obvious to one of ordinary skill in the art to provide a power management setup window in which the power saving standby mode is enabled. Watts teaches that the power saving standby mode may be user enabled [col. 4, lines 10-12], and that the Windows NT operating system is in view [col. 4, lines 53-57]. Additionally, at the time of the invention of Watts, the Windows operating systems were well-known in the art.

Regarding claim 12, Watts teaches that a predetermined time is set to enter the power saving standby mode [col. 4, lines 10-13].

Regarding claim 14, Yamaki/Park teaches the limitations of claim 14 as recited in claim 1. Park also teaches storing the operating state to the system memory when a normal mode is selected [Fig. 4].

Regarding claim 16, Park teaches that the flash memory is a USB device.

Regarding claim 17, Yamaki teaches that the storing of the operating state is performed in a BIOS [col. 11, lines 46-51].

Art Unit: 2115

Regarding claim 18, Yamaki/Watts teaches a method with steps comprising [Watts Fig 3a, 3b]:

copying an operating state data stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated; and

copying the operating state data back to the system memory when a normal mode of the computer system is activated.

Additionally, Yamaki teaches a power management controller to control a power supply [power supply controller 16].

Regarding claim 19, Watts teaches that the normal mode of the computer system is activated without a booting process [col. 2, lines 41-45].

Regarding claim 20, Yamaki/Watts teaches a computer system comprising:

a system memory [Yamaki Fig. 2, system memory 13];

a power management controller to control a supply power to the system [Yamaki Fig. 2, power supply controller 16];

a flash memory [Watts Fig. 3a]; and

a BIOS of the computer system storing an operating state to the flash memory and cutting power to the system [col. 11, lines 46-51].

### ***Conclusion***

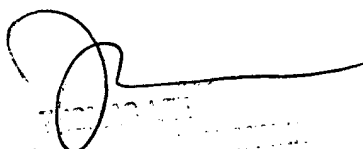
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

Art Unit: 2115

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae  
Patent Examiner  
Art Unit 2115  
[ji.bae@uspto.gov](mailto:ji.bae@uspto.gov)  
571-272-7181



10/23/2013  
Ji H. Bae  
Patent Examiner  
Art Unit 2115